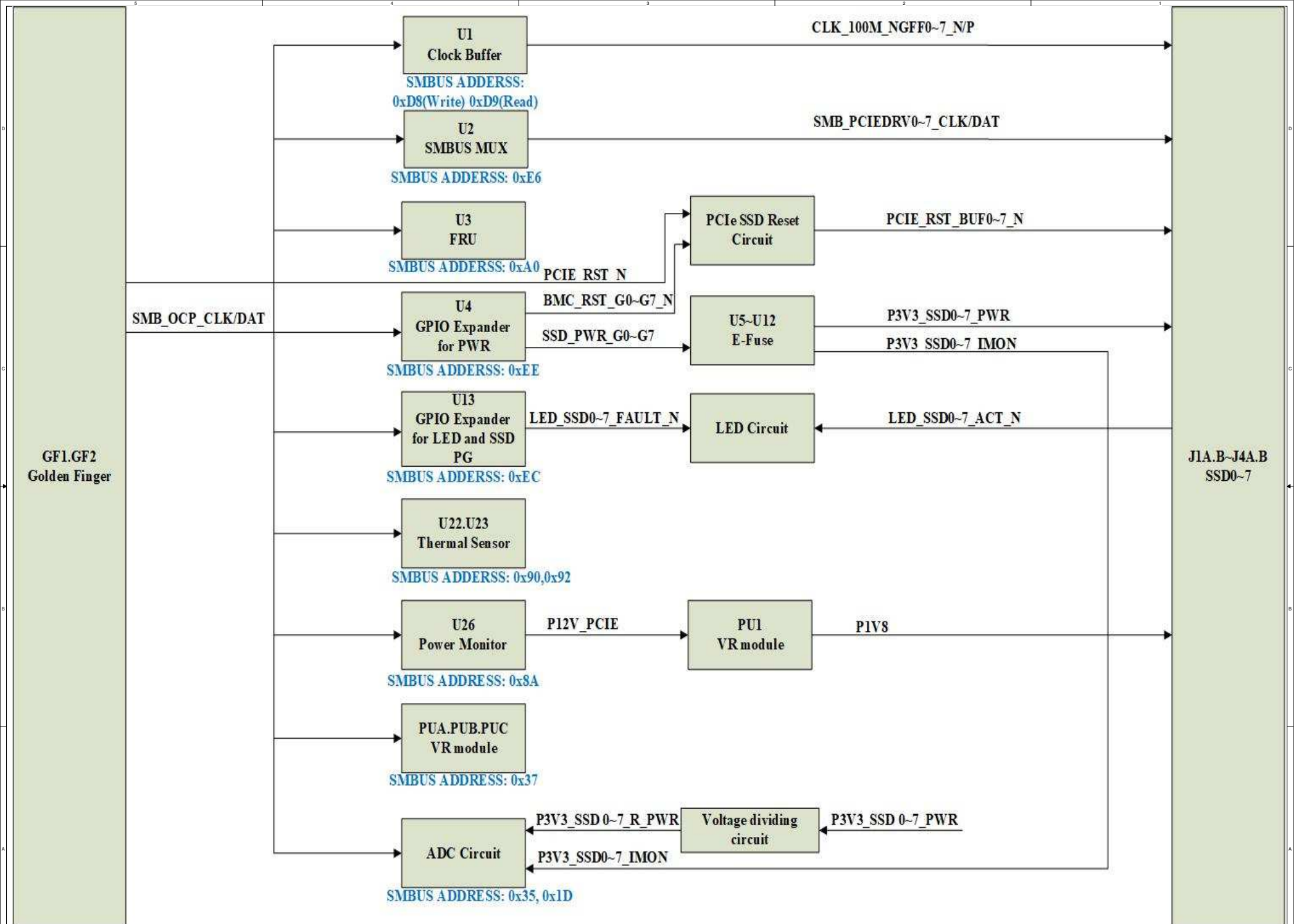


# FOCE IOX M.2 Carrier Card

PCB REV: C  
PCBA REV:  
SCH Rev: V01  
LAST UPDAE: 2020/11/27

# INDEX

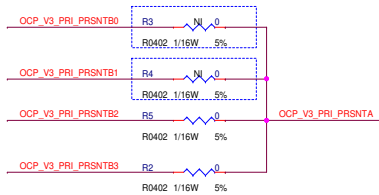
- 1 Cover Page
- 2 Page Index
- 3 Block Diagram
- 4 Primary Gold Finger
- 5 Secondary Gold Finger
- 6 M.2 SSD Slot0/1
- 7 M.2 SSD Slot2/3
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- 16 LED Circuit1
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- 21 VR P3V3 SSD
- 22 P1V8
- 23 ADC Circuit
- 24 Dummy Symbol
- 25 Loss Coupon
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**Block Diagram**

| PRSNT[3:0] | BIF  |
|------------|------|
| 0111       | 1x16 |
| 0110       | 2x8  |
| 0011       | 4x4  |

#### PRSNT DETECT



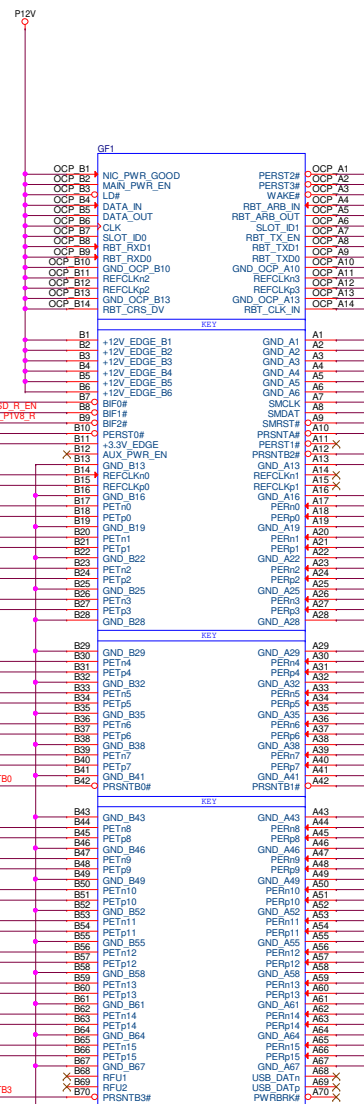
[19] PCIE SMB LEVEL ALERT N  
[4,21] P3V3\_SSD\_EN  
[22] PWRGD\_PIV6

M.2 SSD0

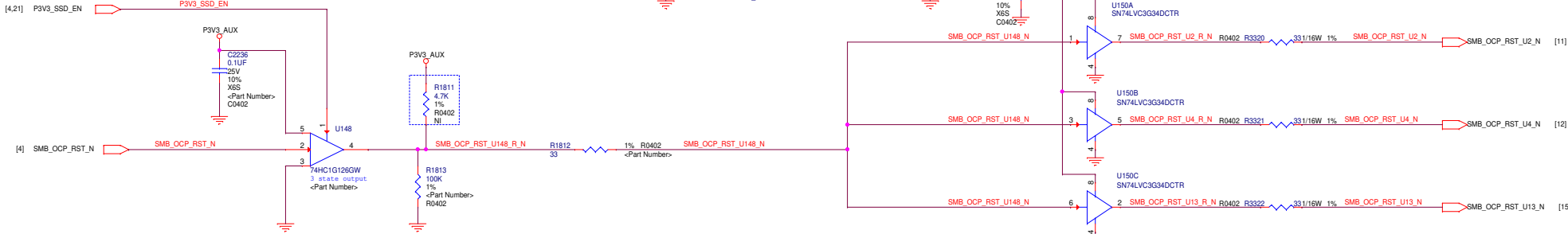
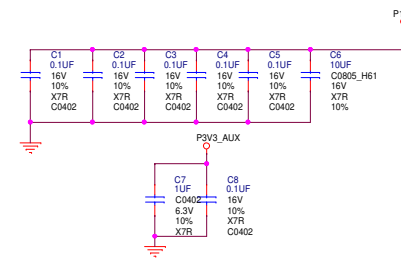
M.2 SSD1

M.2 SSD2

M.2 SSD3



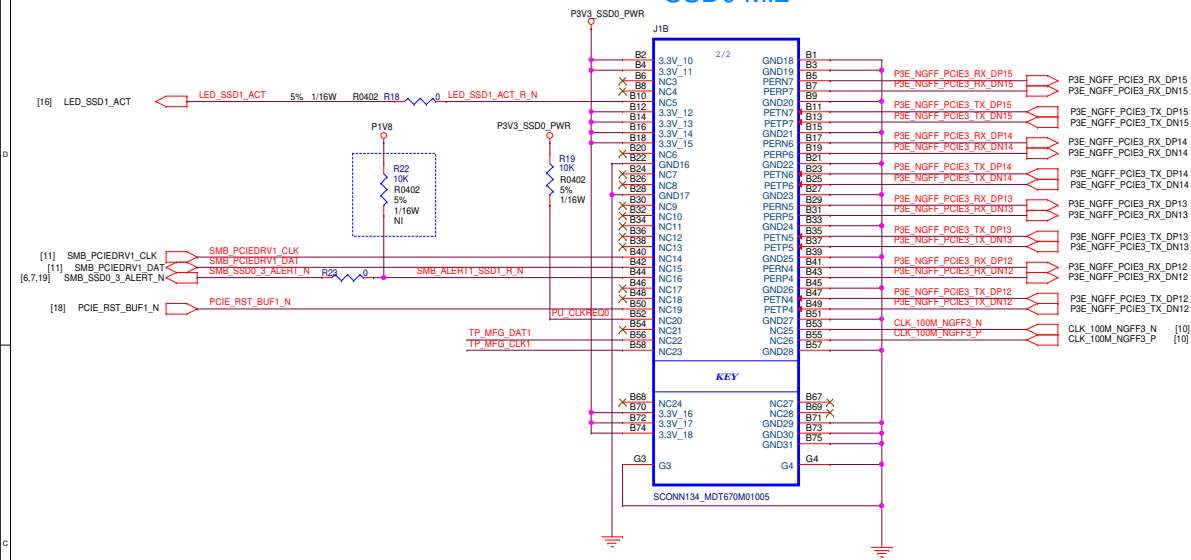
Place caps close to GF1 power pins



Primary Gold Finger

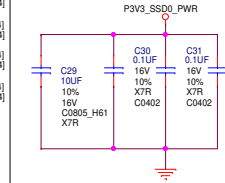


## SSD0 M.2

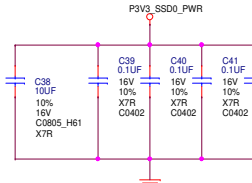


Place caps close to J1B power pins

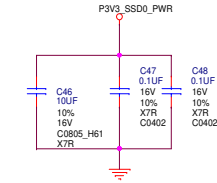
PLACE CLOSE TO PINS 70,72,74



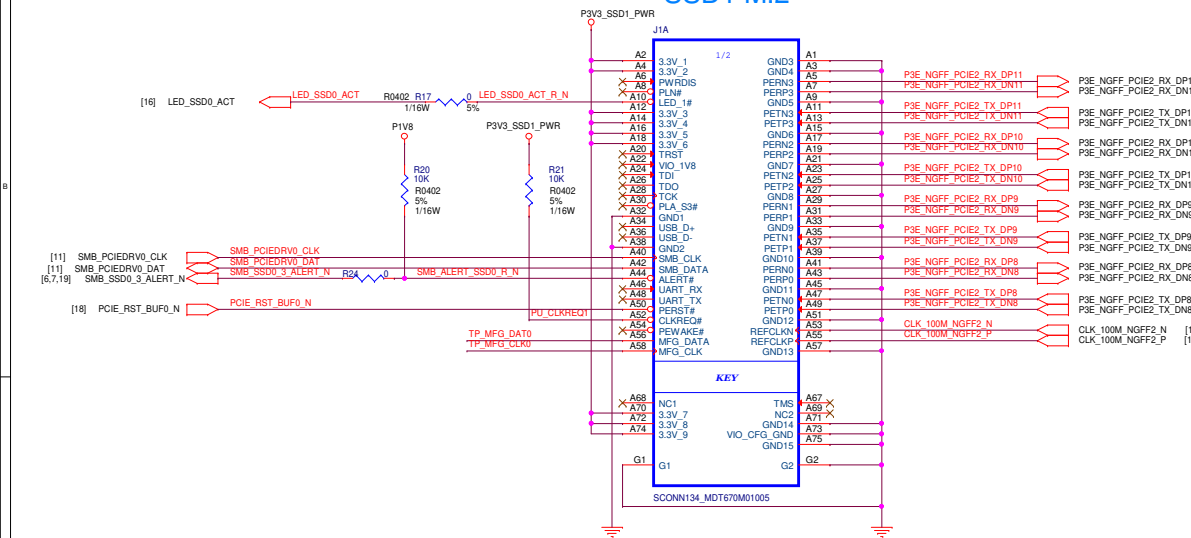
PLACE CLOSE TO PINS 12,14,16,18



PLACE CLOSE TO PINS 2&4

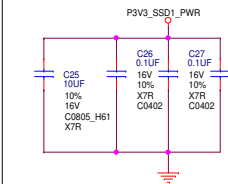


## SSD1 M.2

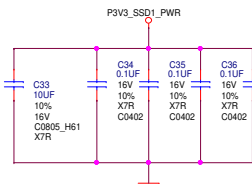


Place caps close to J1A power pins

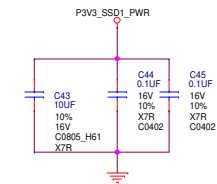
PLACE CLOSE TO PINS 70,72,74



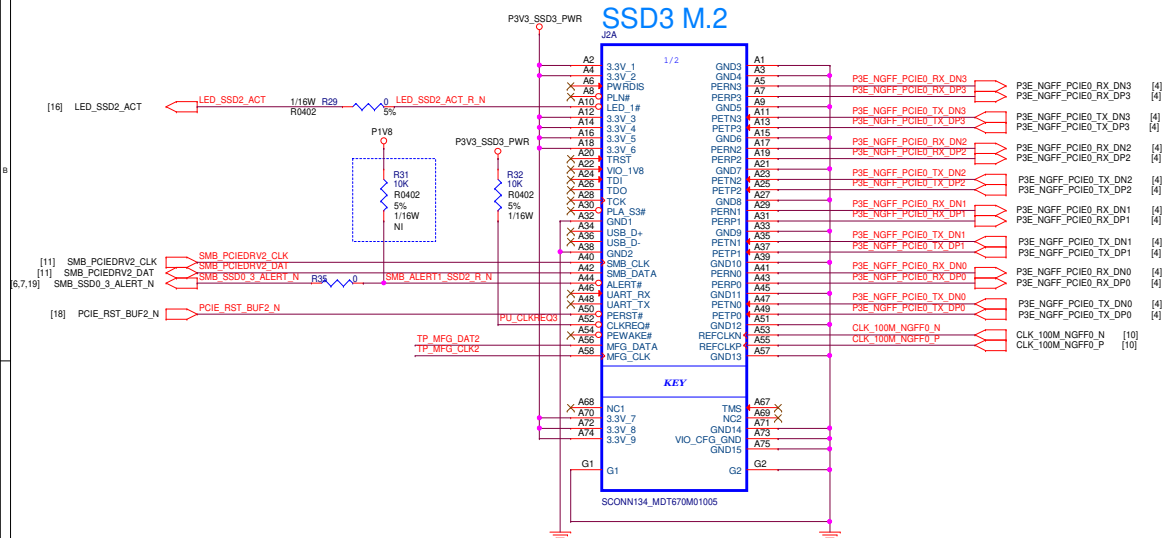
PLACE CLOSE TO PINS 12,14,16,18



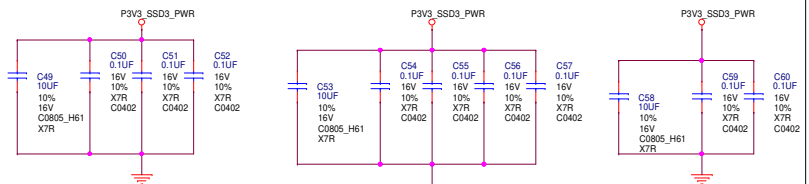
PLACE CLOSE TO PINS 2&4



## SSD3 M.2



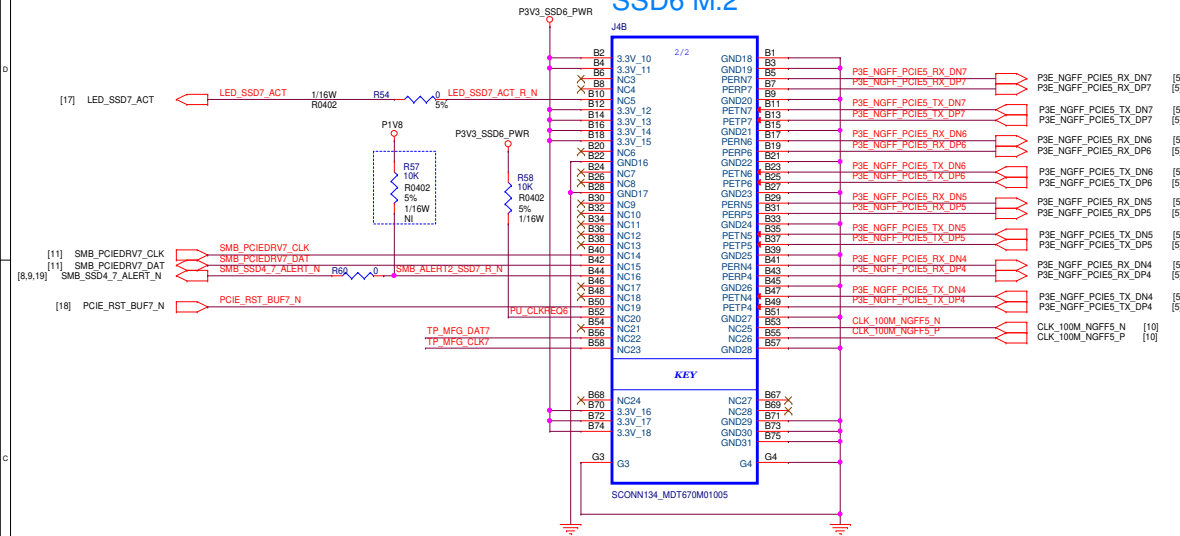
PLACE CLOSE TO PINS 2&4



Rev  
M02  
of 26



## SSD6 M.2

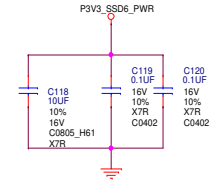
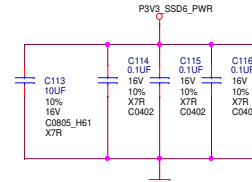
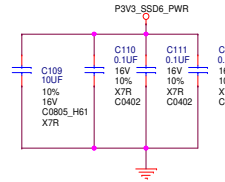


Place caps close to J4B power pins

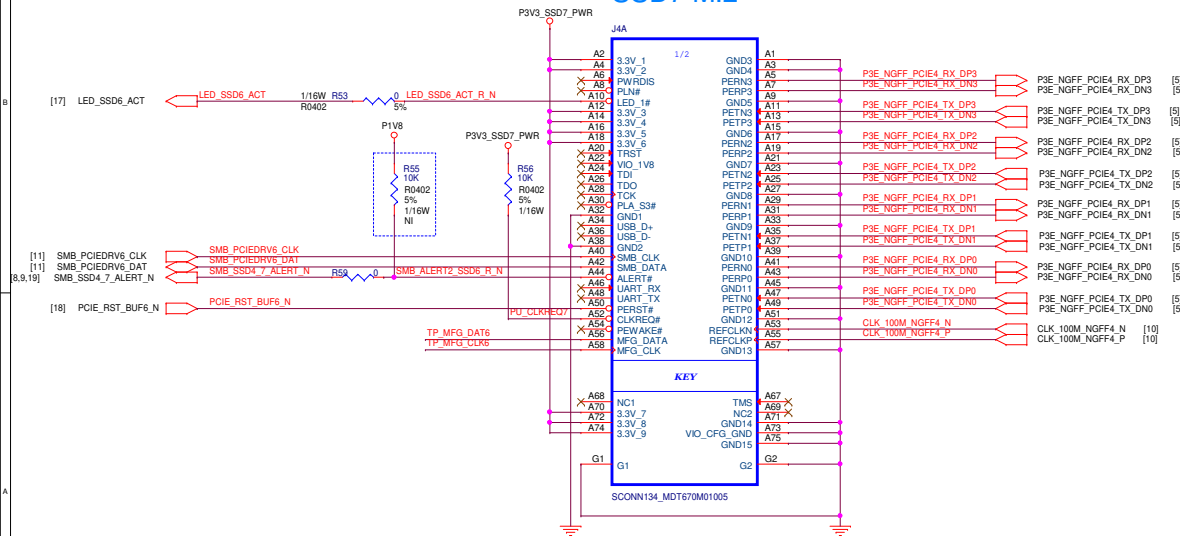
PLACE CLOSE TO PINS 70,72,74

PLACE CLOSE TO PINS 12,14,16,18

PLACE CLOSE TO PINS 2&4



## SSD7 M.2

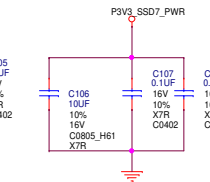
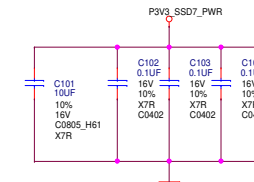
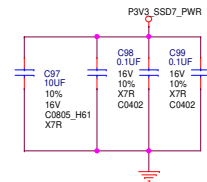


Place caps close to J4A power pins

PLACE CLOSE TO PINS 70,72,74

PLACE CLOSE TO PINS 12,14,16,18

PLACE CLOSE TO PINS 2&4



PLL Operating Mode Table

| HiBW_BypM_LoBW# | MODE      |
|-----------------|-----------|
| Low             | PLL Lo BW |
| Mid             | Bypass    |
| High            | PLL Hi BW |

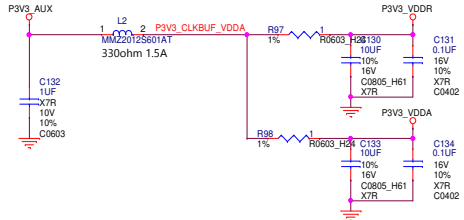
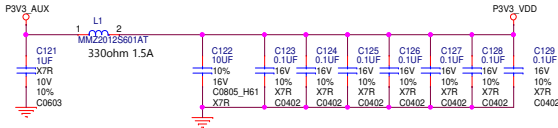
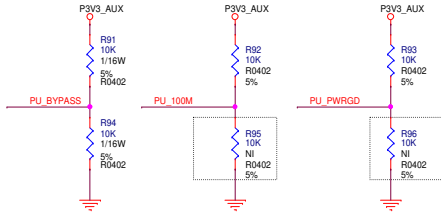
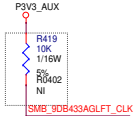
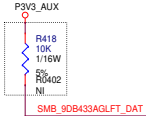
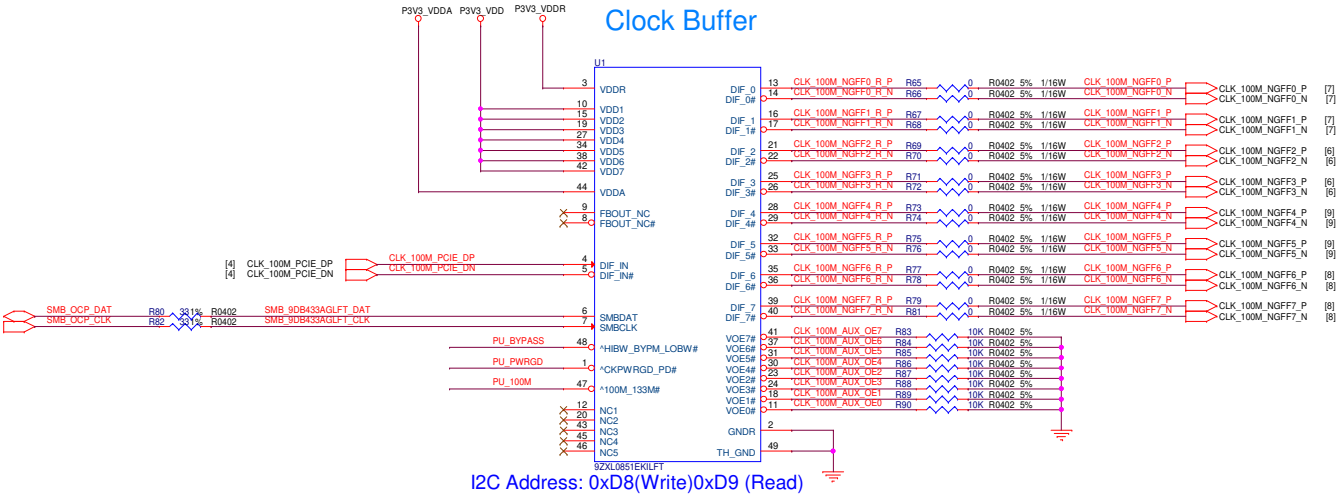
NOTE: PLL is OFF in Bypass Mode

PLL Operating Mode Readback Table

| HiBW_BypM_LoBW# | Byte0, bit 7 | Byte 0, bit 6 |
|-----------------|--------------|---------------|
| Low (Low BW)    | 0            | 0             |
| Mid (Bypass)    | 0            | 1             |
| High (High BW)  | 1            | 1             |

SMBus Address

| Address | + Read/Write bit |
|---------|------------------|
| 1101100 | X                |



Clock Buffer

# PCA9846 Address Define

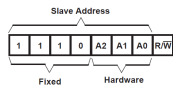
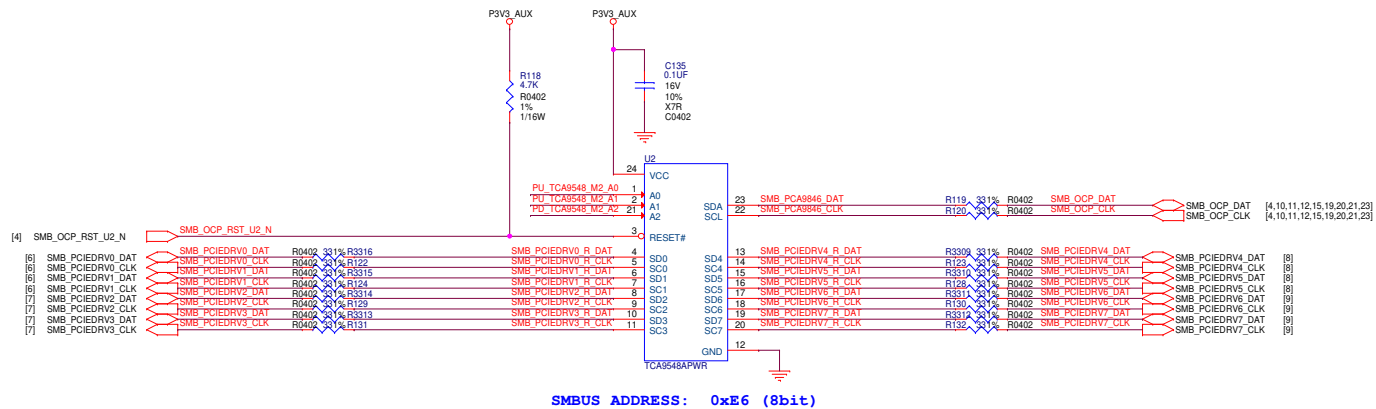
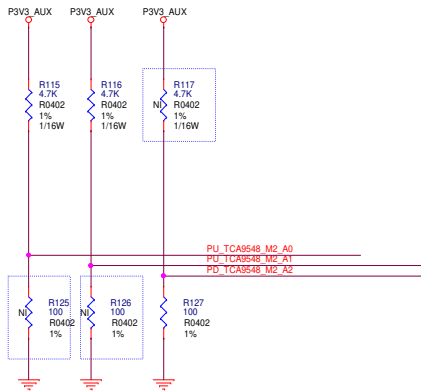
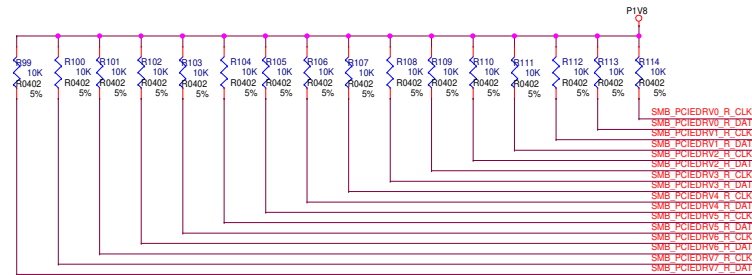


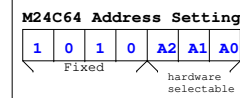
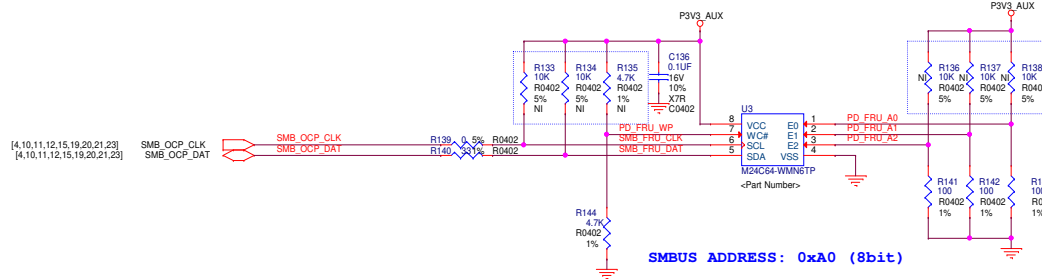
Figure 4. TCA9548A Address

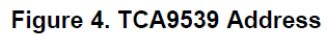
Table 1. Address Reference

| INPUTS |    |    | I <sup>2</sup> C BUS SLAVE ADDRESS |
|--------|----|----|------------------------------------|
| A2     | A1 | A0 |                                    |
| L      | L  | L  | 112 (decimal), 70 (hexadecimal)    |
| L      | L  | H  | 113 (decimal), 71 (hexadecimal)    |
| L      | H  | L  | 114 (decimal), 72 (hexadecimal)    |
| L      | H  | H  | 115 (decimal), 73 (hexadecimal)    |
| H      | L  | L  | 116 (decimal), 74 (hexadecimal)    |
| H      | L  | H  | 117 (decimal), 75 (hexadecimal)    |
| H      | H  | L  | 118 (decimal), 76 (hexadecimal)    |
| H      | H  | H  | 119 (decimal), 77 (hexadecimal)    |



## FRU





### Figure 4. TCA9539 Address

| INPUTS |    | I <sup>2</sup> C BUS SLAVE ADDRESS |
|--------|----|------------------------------------|
| A1     | A0 |                                    |
| L      | L  | 116 (decimal), 74 (hexadecimal)    |
| L      | H  | 117 (decimal), 75 (hexadecimal)    |
| H      | L  | 118 (decimal), 76 (hexadecimal)    |
| H      | H  | 119 (decimal), 77 (hexadecimal)    |



MAX=6A  
OCP=8.96A

```

TIMER setting
3.9nF sets 2 ms delay
47nF sets 20 ms delay

```

| RETRY_DLY    | NRETRY       | DEVICE STATE             |
|--------------|--------------|--------------------------|
| Short to GND | X            | LATCH OFF                |
| OPEN         | open         | 4 auto-retries           |
| OPEN         | Short to GND | Infinite number of retry |

MAX=6A

OCF=8.96A

120570T

QMO-disable the 120570T function

Current scale setting

750 Ohm sets 185mV/A

Output voltage allow rate setting

100mV sets 0.80V/mA

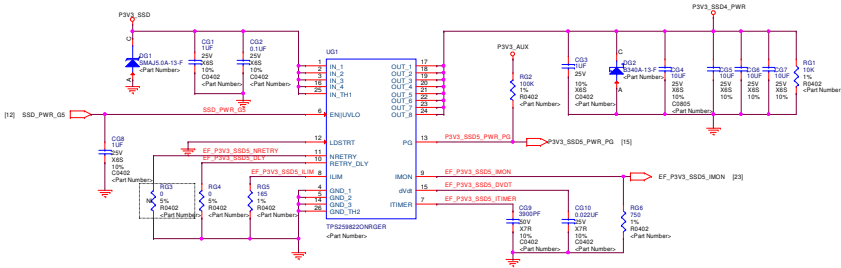
250mV sets 0.21V/mA

ITIMER setting

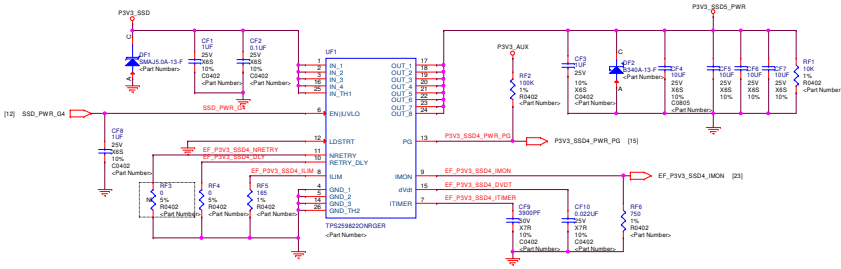
3.9mV sets 2 ms delay

47mV sets 20 ms delay

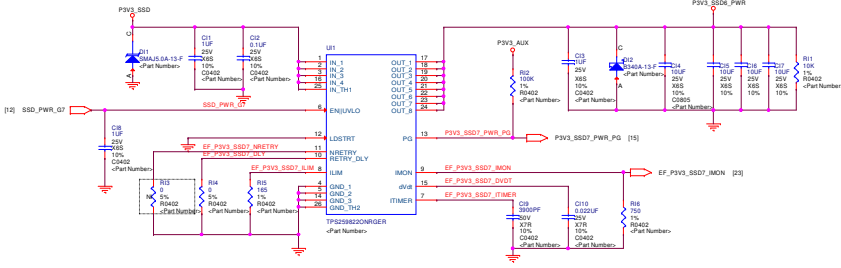
### PWR for SSD4



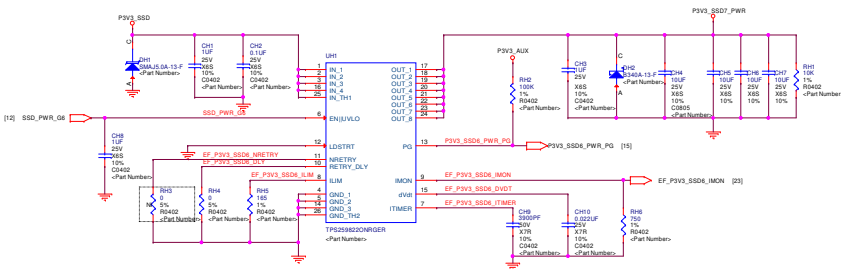
### PWR for SSD5



### PWR for SSD6



### PWR for SSD7



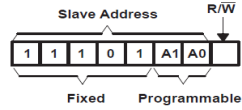
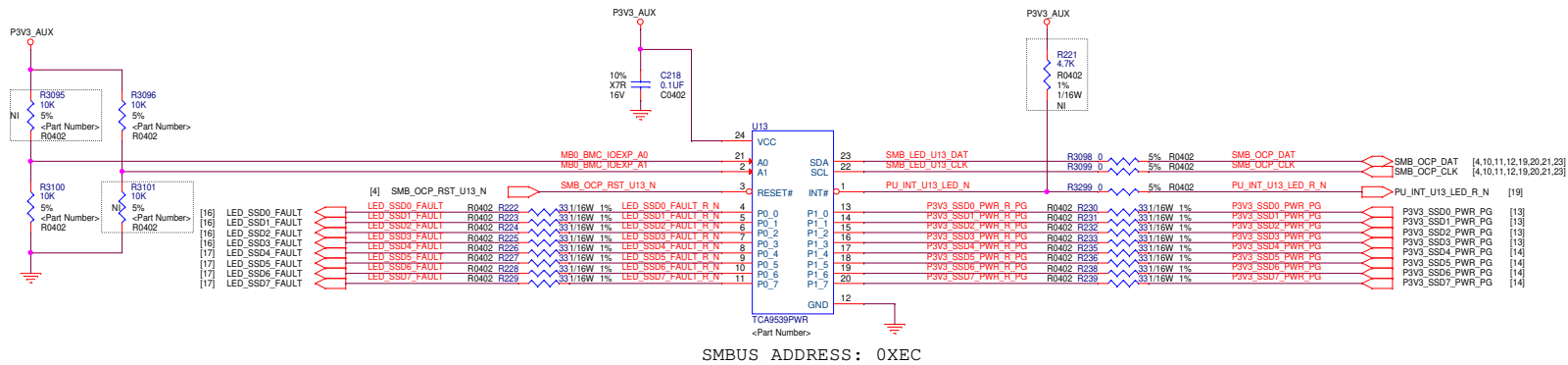


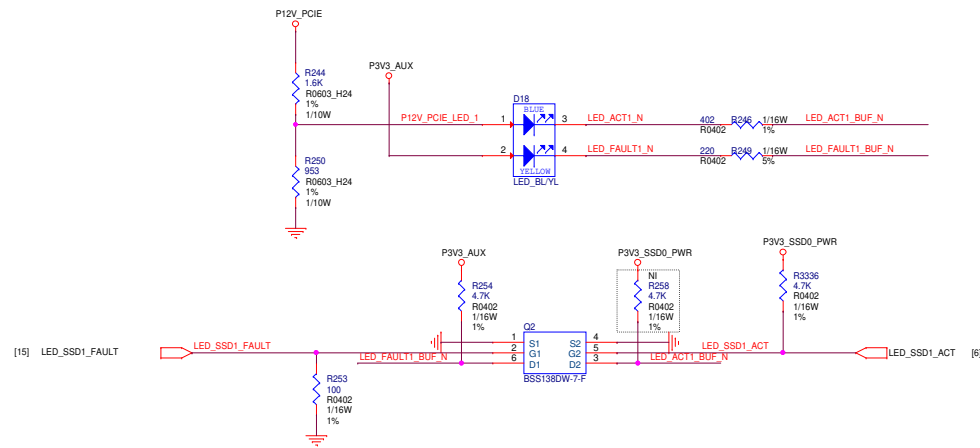
Figure 4. TCA9539 Address

# Address Reference

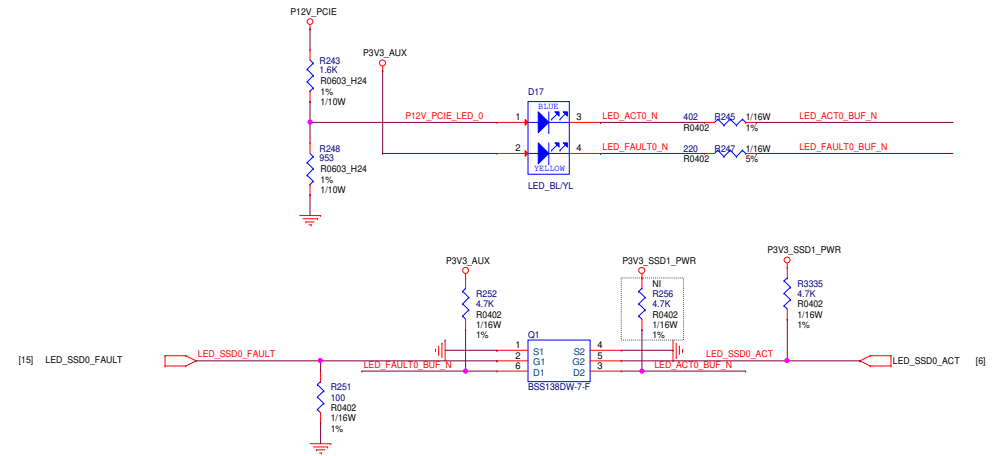
| INPUTS |    | I <sup>2</sup> C BUS SLAVE ADDRESS |
|--------|----|------------------------------------|
| A1     | A0 |                                    |
| L      | L  | 116 (decimal), 74 (hexadecimal)    |
| L      | H  | 117 (decimal), 75 (hexadecimal)    |
| H      | L  | 118 (decimal), 76 (hexadecimal)    |
| H      | H  | 119 (decimal), 77 (hexadecimal)    |



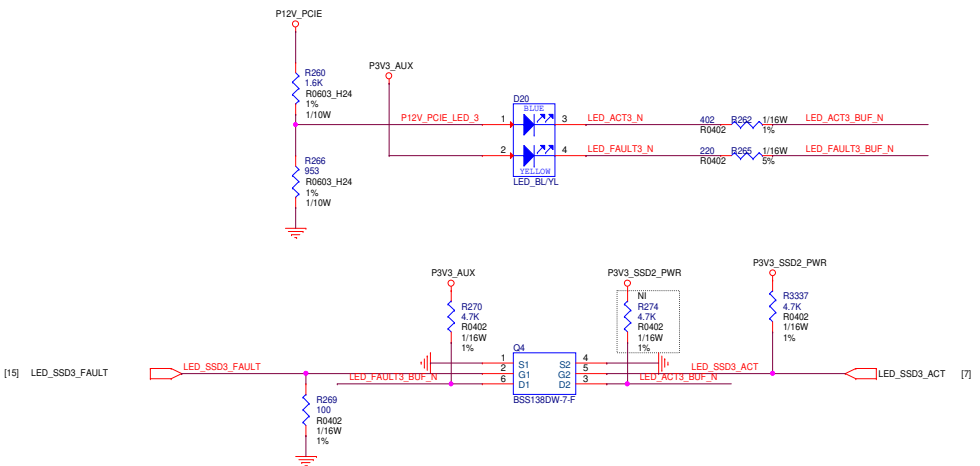
## LED for SSD0



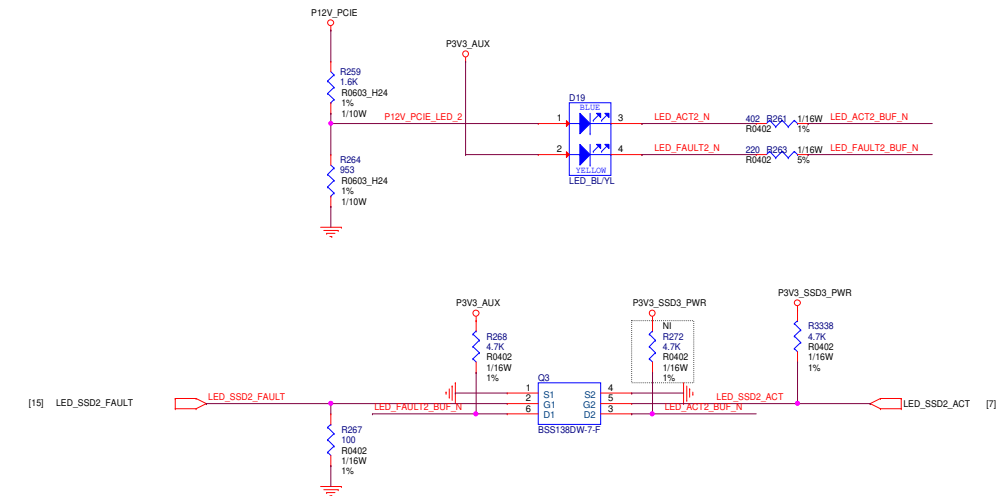
## LED for SSD1



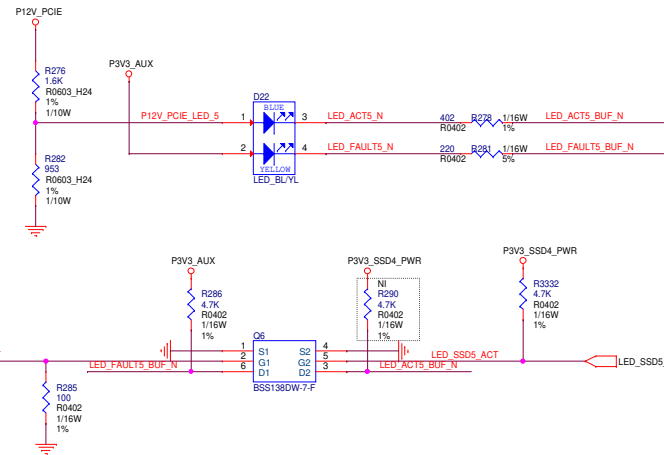
## LED for SSD2



## LED for SSD3



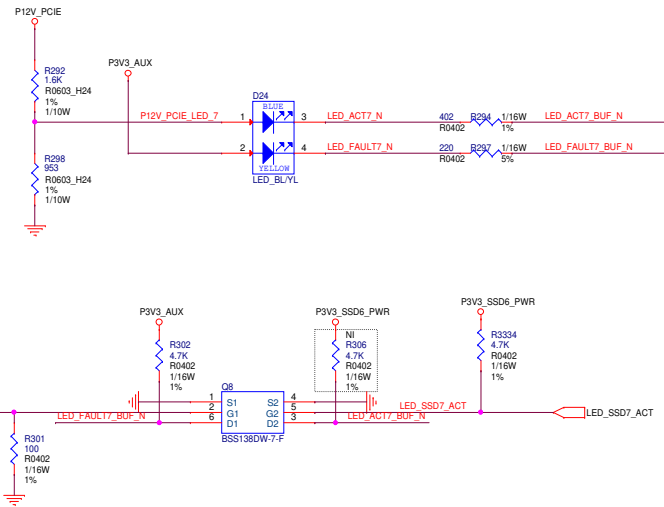
## LED for SSD4



[15] LED\_SSD5\_FAULT

[8]

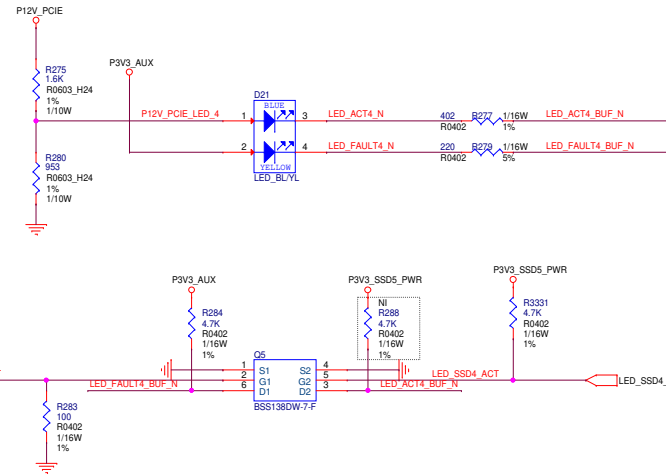
## LED for SSD6



[15] LED\_SSD7\_FAULT

[9]

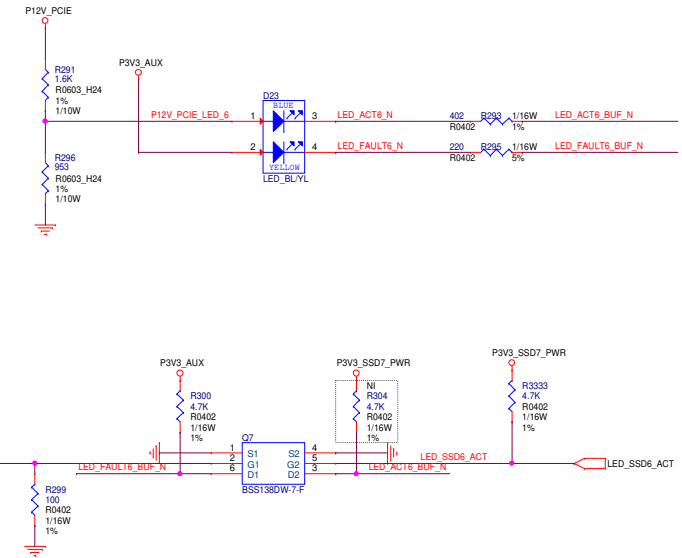
## LED for SSD5



[15] LED\_SSD4\_FAULT

1

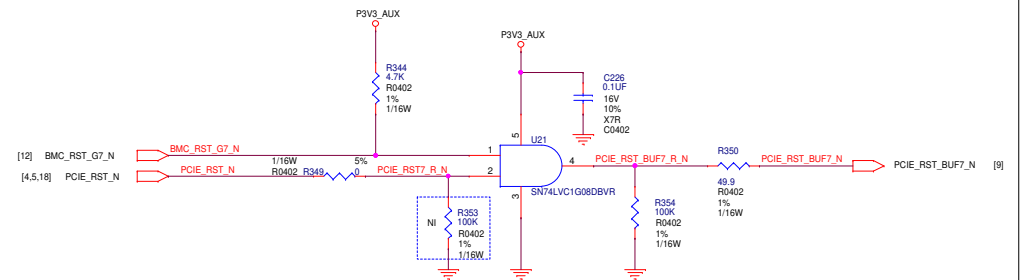
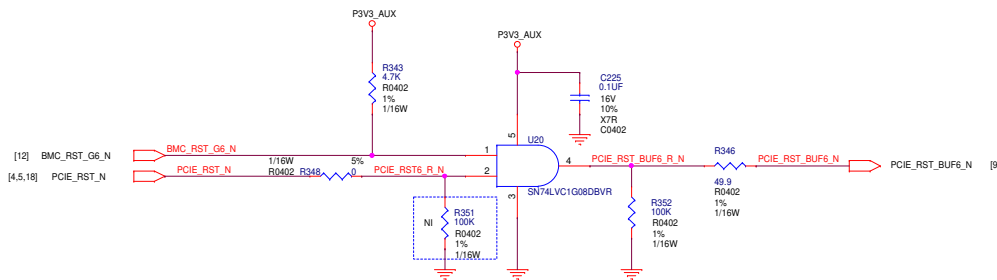
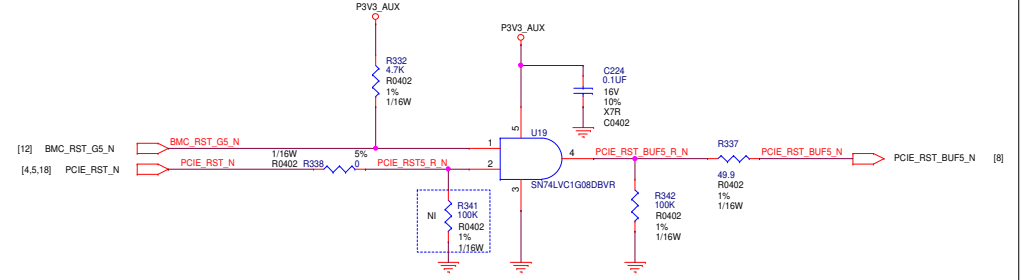
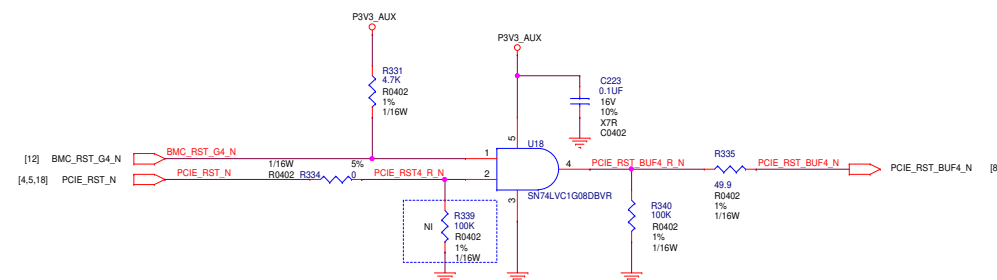
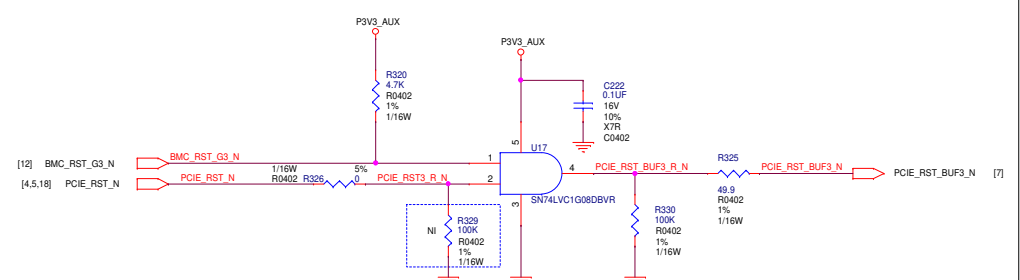
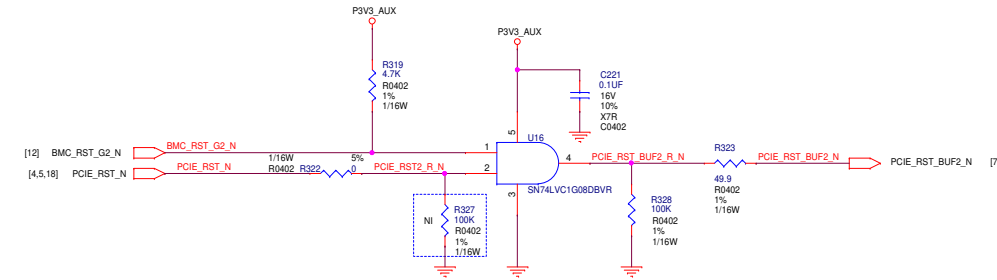
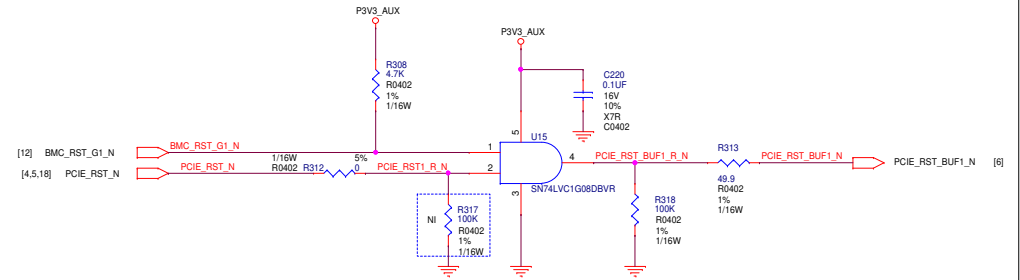
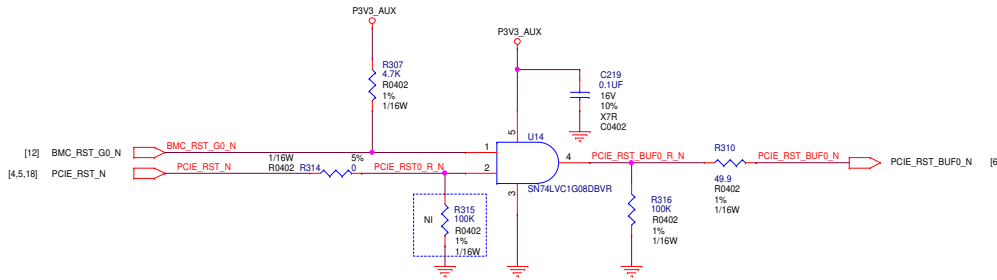
## LED for SSD7



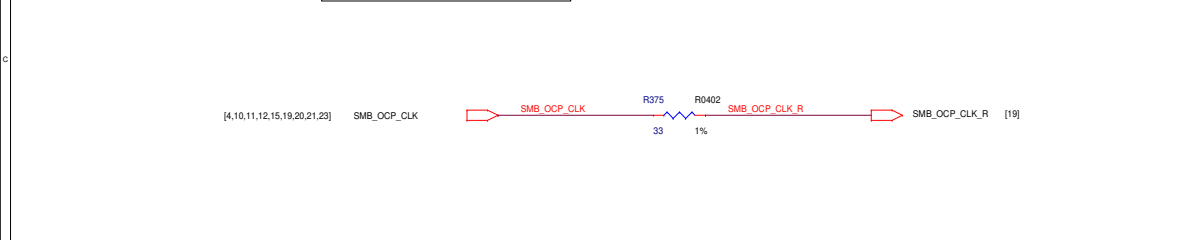
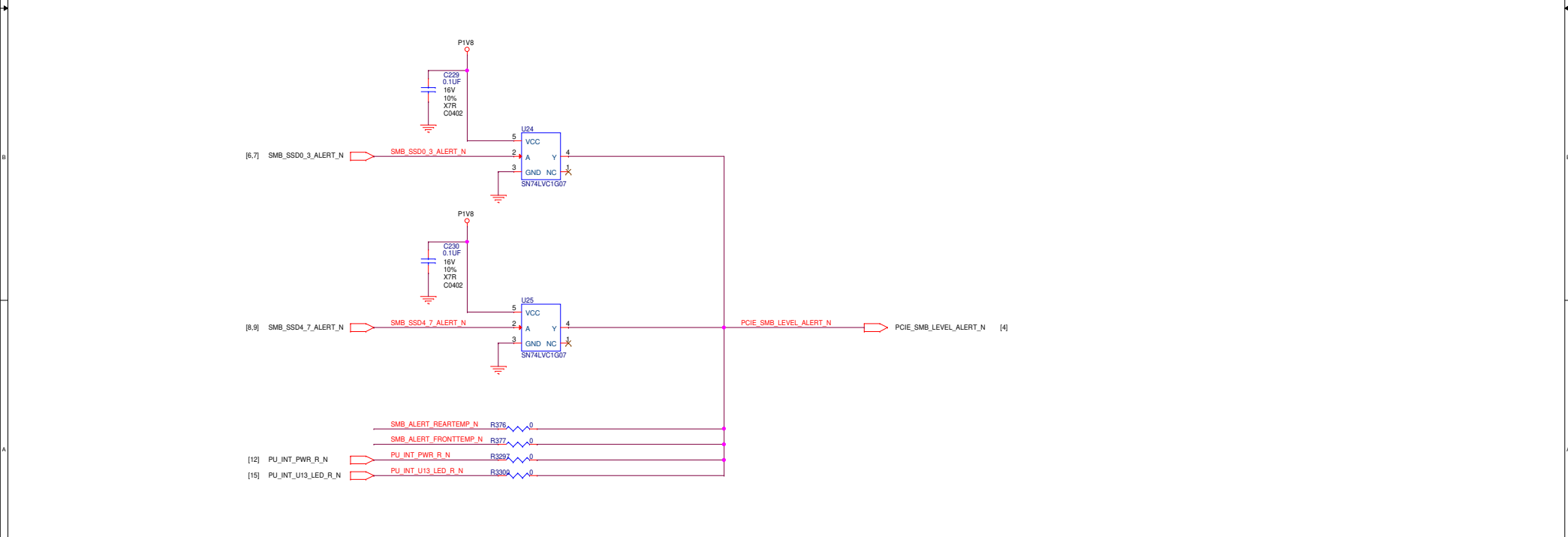
[15] LED\_SSD6\_FAULT

CT

# PCIE SSD RESET CIRCUIT

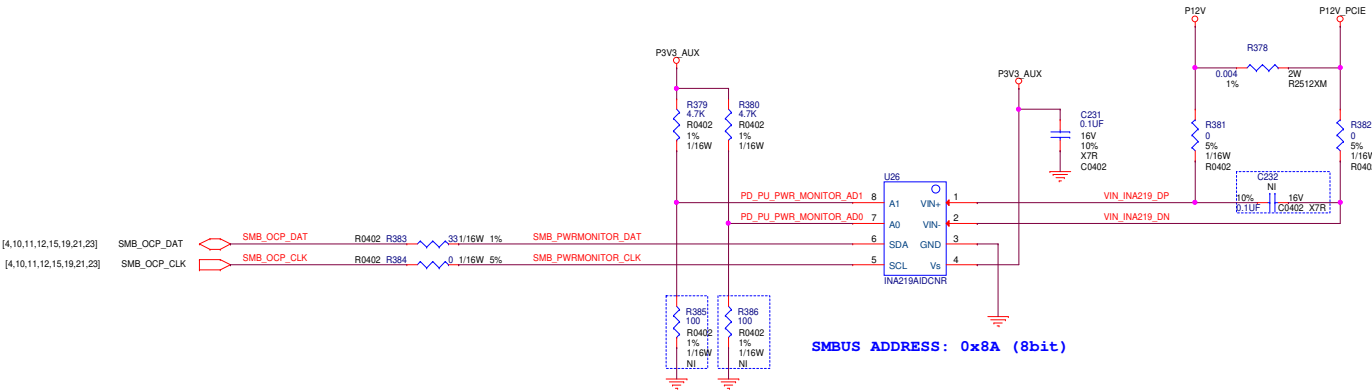


## PCIE SSD RESET CIRCUIT

[illegible][illegible]

**Thermal Sensor**

| A1              | A0              | SLAVE ADDRESS |
|-----------------|-----------------|---------------|
| GND             | GND             | 1000000       |
| GND             | V <sub>S+</sub> | 1000001       |
| GND             | SDA             | 1000010       |
| GND             | SCL             | 1000011       |
| V <sub>S+</sub> | GND             | 1000100       |
| V <sub>S+</sub> | V <sub>S+</sub> | 1000101       |
| V <sub>S+</sub> | SDA             | 1000110       |
| V <sub>S+</sub> | SCL             | 1000111       |
| SDA             | GND             | 1001000       |
| SDA             | V <sub>S+</sub> | 1001001       |
| SDA             | SDA             | 1001010       |
| SDA             | SCL             | 1001011       |
| SCL             | GND             | 1001100       |
| SCL             | V <sub>S+</sub> | 1001101       |
| SCL             | SDA             | 1001110       |
| SCL             | SCL             | 1001111       |

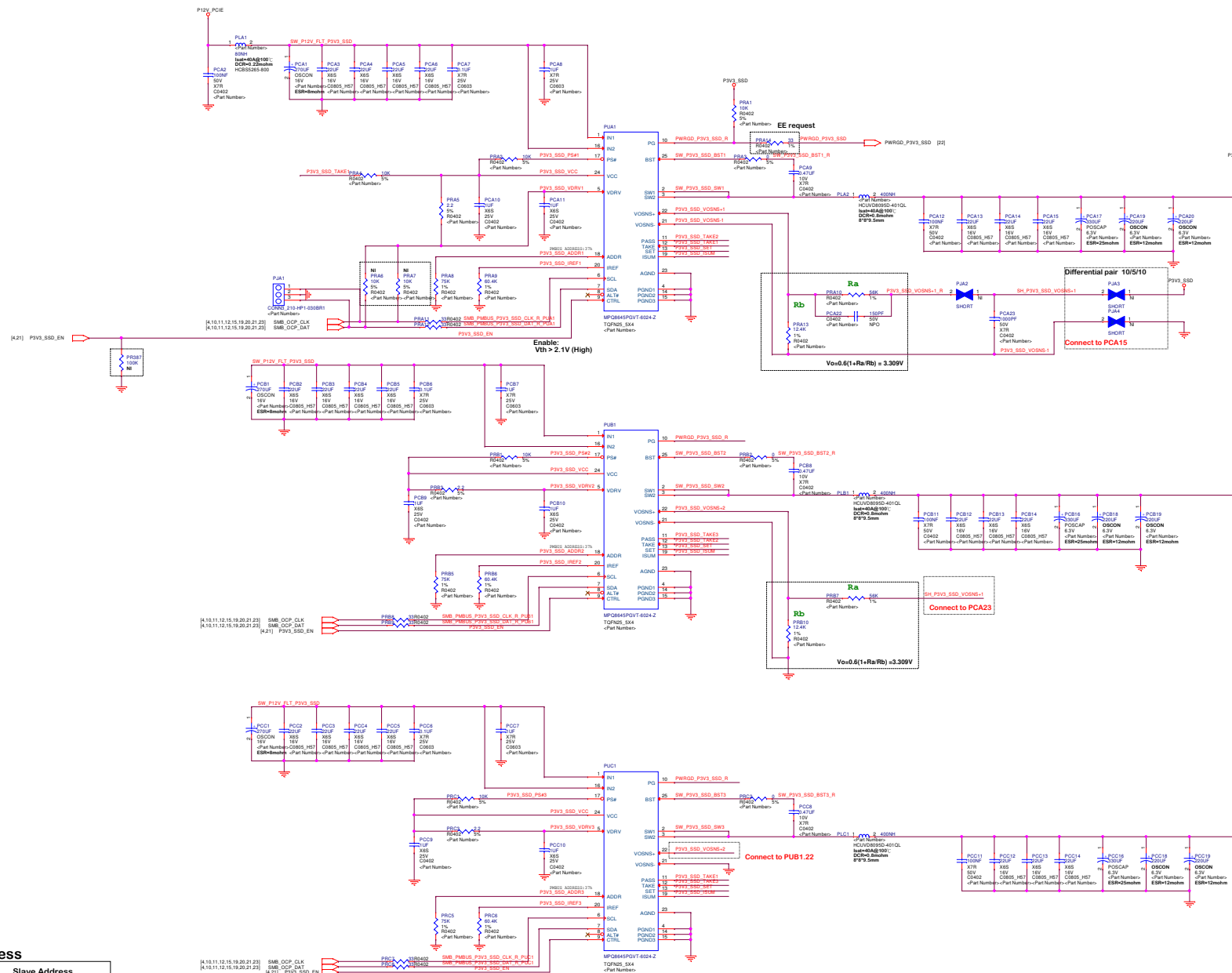


### Design specification

Vout = 3.3 V ±5%  
Vout Ripple & Noise <100 mV  
Vout Tolerance = ±165mV / -165 mV

Iout TDC = 40A  
Iout MAX = 52A (40A-52A for 20us)  
Iout OCP = 62.4 A (Max × 1.2)  
Load Step = 40A-52A for 20us, period time=1ms  
Slew Rate = 12 A/us

Fsw = 600K Hz  
Efficiency > 85% @TDC  
Multi-phase constant-on-time (MCOT) control



### PMBus Address

| RADDR(kohm) | Slave Address (R_IREF=60.4kohm) |
|-------------|---------------------------------|
| 75          | 37h                             |

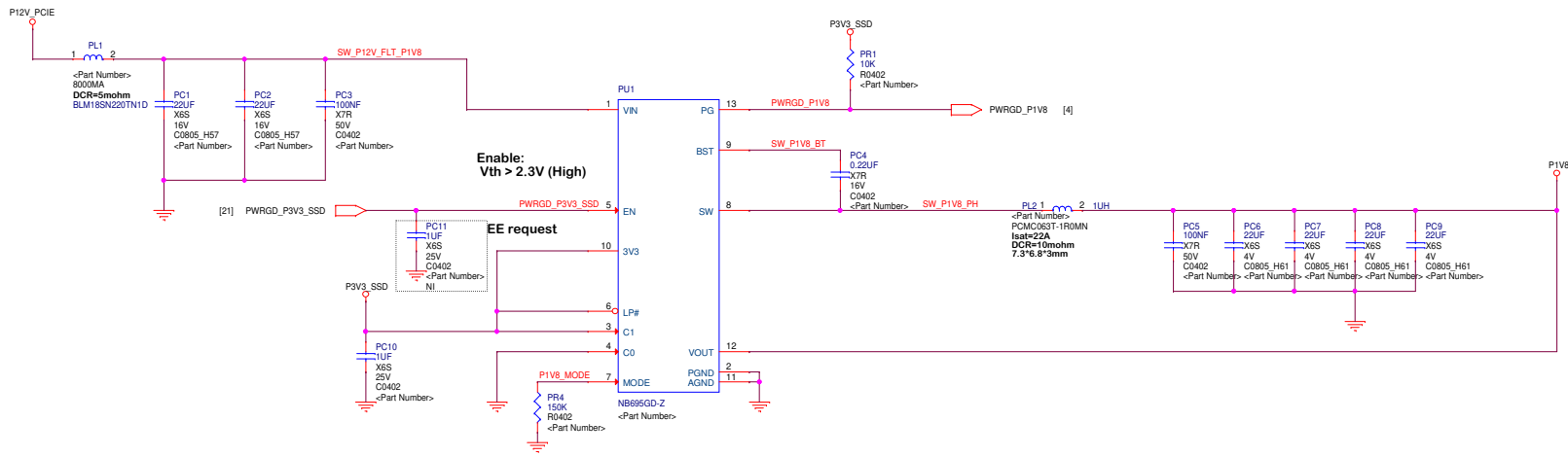
### VR P3V3 SSD

Design specification

Vout = 1.8V  
Vout Ripple & Noise < 90 mV (5%)  
Vout Tolerance = +90 mV / -90 mV

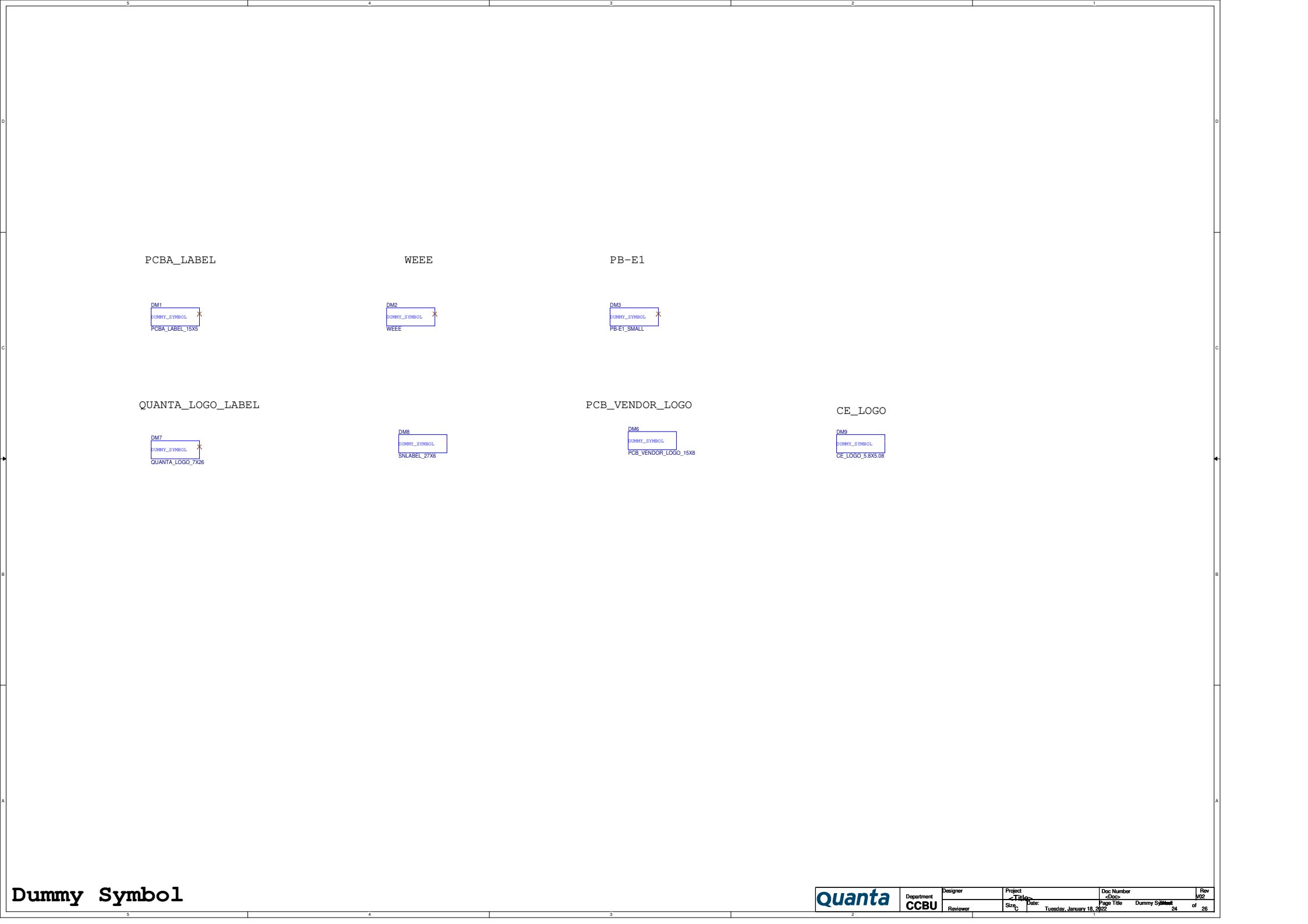
Iout TDC = 2A  
Iout MAX = 2A  
Iout OCP = 3.5 A (Spec)  
Load Step = 1 A (TBD)  
Slew Rate = 2.5A/us (TBD)

Fsw = 750k Hz  
Efficiency > 85% @TDC  
COT Control Mode



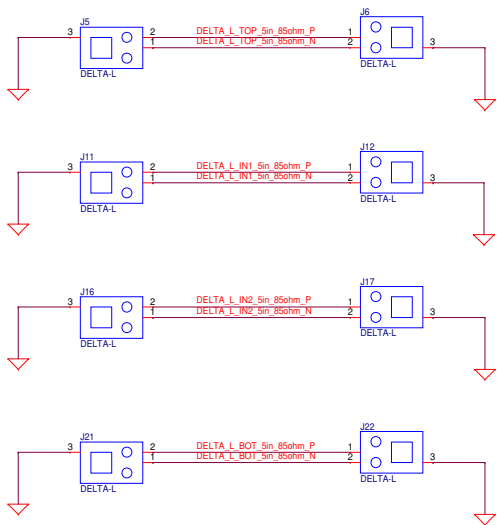
ROUTE ALL ADC NETS AT 10 MILLS WIDE

| CH. | MODE 0 | MODE 1 | MODE 2          | MODE 3 |
|-----|--------|--------|-----------------|--------|
| 1   | IN0    | IN0    | IN0 (1 and 2)   | IN0    |
| 2   | IN1    | IN1    | IN1 (1 and 2)   | IN1    |
| 3   | IN2    | IN2    | IN2 (1 and 2)   | IN2    |
| 4   | IN3    | IN3    | IN3 (1 and 2)   | IN3    |
| 5   | IN4    | IN4    | IN4 (1 and 2)   | IN4    |
| 6   | IN5    | IN5    | IN5 (1 and 2)   | IN5    |
| 7   | IN6    | IN6    | IN6 (1 and 2)   | IN6    |
| 8   | IN7    | IN7    | IN7 (1 and 2)   | IN7    |
| 9   | IN8    | IN8    | IN8 (1 and 2)   | IN8    |
| 10  | IN9    | IN9    | IN9 (1 and 2)   | IN9    |
| 11  | IN10   | IN10   | IN10 (1 and 2)  | IN10   |
| 12  | IN11   | IN11   | IN11 (1 and 2)  | IN11   |
| 13  | IN12   | IN12   | IN12 (1 and 2)  | IN12   |
| 14  | IN13   | IN13   | IN13 (1 and 2)  | IN13   |
| 15  | IN14   | IN14   | IN14 (1 and 2)  | IN14   |
| 16  | IN15   | IN15   | IN15 (1 and 2)  | IN15   |
| 17  | IN16   | IN16   | IN16 (1 and 2)  | IN16   |
| 18  | IN17   | IN17   | IN17 (1 and 2)  | IN17   |
| 19  | IN18   | IN18   | IN18 (1 and 2)  | IN18   |
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| 237 | IN236  | IN236  | IN236 (1 and 2) | IN236  |
| 238 | IN237  | IN237  | IN237 (1 and 2) | IN237  |
| 239 | IN238  | IN238  | IN238 (1 and 2) | IN238  |
| 240 | IN239  | IN239  | IN239 (1 and 2) | IN239  |
| 241 | IN240  | IN240  | IN240 (1 and 2) | IN240  |
| 242 | IN241  | IN241  | IN241 (1 and 2) | IN2    |

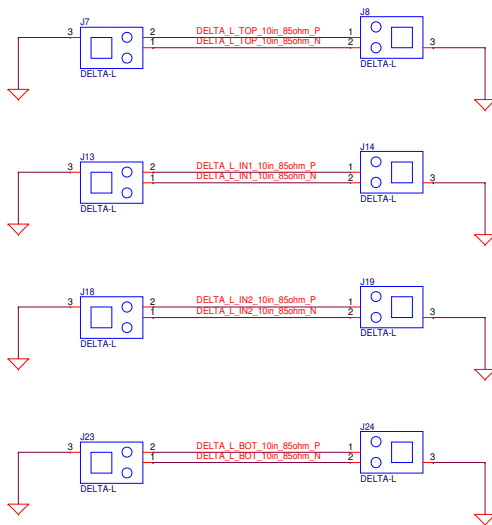


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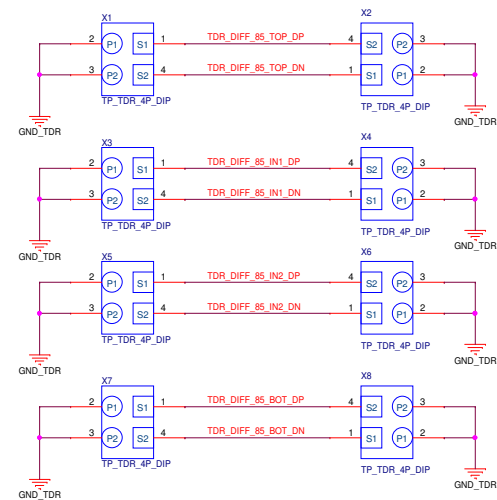
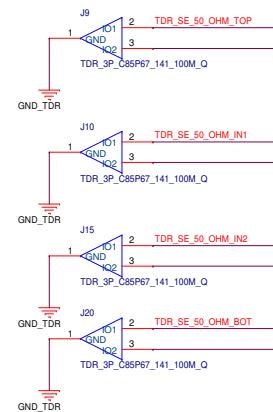
## 5 inch trace



## 10 inch trace



## TDR



SCREW HOLE

